PATENT ATTORNEY DOCKET: N1085-00190
[TS03-0119]

IV. Remarks

A. Summary of Amendments

Claims 1-22 are pending in the present application. Claim 1 has been amended as described in detail below. Claim 16 has been amended to correct its dependency.

Paragraph 9 has been amended to recite certain features of active device 240. Support for this amendment can be found at, for example, Claim 16 of the application as filed.

B. Rejection under 35 U.S.C. §102

1. Rejection Claim 1-4: Staab et al

The Action rejects Claim 1-4 as being anticipated by U.S. Patent No. 5,610,790 to Staab et al.

Claim 1 has been amended to clarify that the second connection "couples said pad to a functional circuit for which said ESD protection is provided." In other words, the second connection is the node that is being protected from ESD, i.e., a node between the resistor and the functional circuit being protected.

Not by way of limitation, but for purposes of explanation, Applicants refer the Examiner to FIG. 2 of the present application, with bolded, annotated comparison to Claim 1. Claim 1 is directed to a circuit for electrostatic discharge (ESD) protection, comprising:

- a low capacitance ESD protection circuit **(circuit 220)** coupled to a pad **(pad 210)** and a ground **(Vss)**;

- a first resistive device **(device 230)**, comprising a first connection coupled to the pad **(pad 210)** and a second connection that couples the pad to a functional circuit **(circuit block 250 including buffer 251, 252 and internal circuit 253)** for which said ESD protection is provided; and

- a second device **(transistor 240)** coupled to the second connection of the first resistive device **(device 230)** and to the ground **(VSS)**.

It is clear from the annotation above that Claim 1 recites the "low capacitance ESD protection circuit coupled to a pad and a ground" as one of three elements, the other two being the recited "resistive device" and "second device." Notwithstanding this, the Examiner seems to have ignored the "low capacitance ESD protection circuit" element.

In rejecting Claim 1, the Examiner first relies on FIG. 1 of Staab. This figure shows an input pad 100 coupled to a resistor 103, which is coupled to integrated circuit logic circuitry 102. A transistor is coupled between ground and the node connecting the resistor 103 and logic circuitry 102. The Examiner does not identify an actual part of FIG. 1 of Staab et al., however, that is a "low capacitance ESD protection circuit coupled to a pad and a ground." Indeed, even a cursory review of FIG. 1 of Staab et al. shows no circuit or device is coupled between the pad 101 and ground (VSS). Further, even though the circuit of Staab et al. includes no capacitor as argued by the Examiner, it does not follow that the circuit includes a low capacitance ESD protection circuit coupled to the pad and ground as claimed. In short, Claim 1 requires the inclusion of an ESD protection circuit to be coupled between the pad and ground, in addition to the recited resistive device and second device, and FIG. 1 of Staab shows no such structure.

The Examiner also makes reference to FIG. 7 of Staab et al. Specifically, the Examiner cites to resistor 712, pad 701, pad 711, ground and second device 703, while stating "[a]gain, the device is low capacitance since no capacitor is in the circuit." First, reference 711 identifies an internal circuit to be protected from ESD, not a pad (Column 7, Lines 1-2). Second, resistor 712 is coupled to pad 701 and to power supply VDD through diode 702. Resistor 712 is not connected to "a second connection that couples the pad to a functional circuit" as claimed. Indeed, pad 710 couples directly to the input of inverter buffer 708. Third, alleged "second device" 703 is not connected between "a second connection that couples the pad to a functional circuit" and ground. Rather, device 703 is coupled to pad 701. Last, as explained above, Claim

1 affirmatively recites "a low capacitance ESD protection circuit coupled to a pad and a ground" in addition to the affirmative recitation of the resistive device and second device. The Examiner has identified no such ESD protection circuit in Fig. 7 that meets this limitation that is provided in addition to the alleged resistive device and second device.

Per the foregoing, it is submitted that Claims 1-4 are not anticipated by Staab et al. and are allowable thereover. Reconsideration and withdrawal of the rejection of these claims are respectfully requested.

C. Rejection under 35 U.S.C. §103

The Action rejects Claim 1-22 as being obvious from U.S. Patent No. 6,690,557 to Hung et al. in view of Staab et al.

In the rejection, the Examiner concludes that it would have been obvious to one of skill in the art to modify the device of FIG. 1 of Hung et al. to add a resistive element between the pad and the buffer. It is respectfully submitted that there is suggestion or motivation in the art to make this modification and any such suggestion impermissibly relies on Applicants' disclosure.

The Examiner relies on the following motivation to combine the disclosures of Hung et al. and Staab et al.: "to reduce the RC delay of signals transmitted from the pad to the buffer [of Hung et al.]." It is respectfully submitted that if one of ordinary skill were to try to reduce RC delay of signals from the input bonding pad of Hung to the input buffer 104 of Hung et al., that person would not add a resistive element between the input pad and the input buffer. Certainly, the existing short circuit connection between the input bonding pad 106 of Hung et al. and the input buffer 104 would produce less RC delay than if the signal were interrupted with a resistive element between the two nodes. Simply, the combination proffered by the Examiner would not work for the Examiner's intended purpose. Indeed, Staab et al. expressly teaches that providing input resistance raises RC delay: "The resistor used in the ESD protection circuit has a lower

resistance than conventional input resistors. As a result, the RC delay of signals transmitted from the pad to the input buffer is greatly reduced." (Column 5, Lines 11-15).

Per the foregoing, it is respectfully submitted that there is no suggestion or motivation in the art of record to combine the teachings of the two references. Therefore, it is submitted that the Examiner has not set forth a *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejection of Claim 1 and Claims 2-7, which depend from Claim 1, are respectfully requested.

Independent Claim 8 is directed to an integrated circuit having a pad, a buffer, an internal circuit and an ESD protection device as discussed above in connection with Claim 1. The Examiner again concludes that it would have been obvious to combine the teachings of Hung et al. with Staab et al. in order to reduce the RC delay of signals transmitted from the pad to the buffer. It is again submitted that this combination would increase the RC delay of the circuit of Hung et al. It is further submitted, therefore, that there is no suggestion or motivation in the art of record to combine the teachings of the two references. Accordingly, reconsideration and withdrawal of the rejection of Claim 8 and Claims 9-16, which depend from Claim 1, are respectfully requested.

Independent Claim 17 is directed to a method of protecting an internal circuit from ESD and includes the step of using an additional circuit operatively coupled intermediate the ESD protection circuit and the functional circuit to effect a voltage drop between the pad and the function circuit. The Examiner again relies on the combination of Hung et al. and Staab et al. and provides the same reasoning discussed above for making the combination. Per the reasons set forth above, it is submitted that there is no suggestion or motivation to combine the teaching to provide the method of Claim 17. Accordingly, it is submitted that Claim 17 is not obvious from the cited combination and reconsideration and withdrawal of the rejection of Claim 17 and Claims 18-22, which depend from Claim 17, are requested.

PATENT ATTORNEY DOCKET: N1085-00190
[TS03-0119]

V. Conclusion

In view of the foregoing remarks and amendments, Applicant(s) submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

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